Amendments to the Specification:

Amend the specification by inserting a new section before the "Technical Field" as follows:

-- CROSS-REFERENCE TO RELATED APPLICATION

This application is a continuation of pending United States Patent Application No. 10/014,013, filed November 5, 2001. –

Please replace the paragraph beginning on page 5, line 16, with the following amended paragraph:

The major disadvantage of the circuitry used in the burst controller 42' of Figure 2 stems from the number of circuit components the external address bits must be coupled through to generate the internal address bits. Specifically, from the address latch 40, the LA_[S0] S1 signal for the even columns is coupled through [the inverter 152, the NOR-gate 150, the multiplexer 142, the inverter 146, and the multiplexer 110] the multiplexer 110, the driver 120, the adder logic 100. In contrast, the LA_[S0] S1 signal for the odd columns is coupled through only a multiplexer [170] 110. A similar disparity exists between the LA_[S1] S2 signal for the odd columns and the LA_[S1] S2 signal for the even columns. As a result, the internal address bits IA<2:1> for the even columns reach the column decoder 44 (Figure 1) substantially later than the internal address bits IA<2:1> for the odd columns. In addition to this lack of symmetry, the inherent delay in passing the latched address bits LA_[S0] S1 and LA_[S1] S2 through [five] the circuit components unduly delays the time that the column decoder 44 can begin decoding a column address.